

Index of Claims



Application No.

10/066,182

Examiner

TRONG PHAN

Applicant(s)

MCCLURE, DAVID C.

Art Unit

2818

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date									
Final	Original	12/19/03									
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Claim		Date									
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means for placing on an external pad of the apparatus during a test mode of operation a current level corresponding to a voltage level appearing across the ferroelectric capacitor, said means comprising a first transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first conduction terminal coupled to the external pad and a second conduction terminal ~~connected to a voltage reference~~, and a second transistor having a first conduction terminal connected to ~~the external pad~~ a voltage reference and a second conduction terminal connected to the ~~first~~ second conduction terminal of the first transistor, and a means for selectively activating the second transistor during the test mode of operation.

38. (Canceled).

39. (Canceled).

40. (Previously Added) The random access memory device of claim 1, wherein the current level placed on the external pad by the test circuitry is proportional to the voltage level appearing on the at least one bit line.

¹
41. (Previously Added) The method of claim ~~16~~, wherein the current level provided to the pad is proportional to the voltage level appearing on the selected bit line.

42. (Previously Added) The apparatus of claim 22, wherein the current level placed on the external pad is proportional to the voltage level appearing on the at least one bit line.